ADVANCE INFORMATION   TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT   SILICON MONOLITHIC

# TC74VCX16821FT

LOW-VOLTAGE 20-BIT D-TYPE FLIP-FLOP
WITH 3.6V TOLERANT INPUTS AND OUTPUTS

The TC74VCX16821FT is a high performance CMOS 20-bit D-TYPE FLIP-FLOP. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
It is also designed with over voltage tolerant inputs and outputs up to 3.6V.
The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 20-bit operation. The following description applies to each byte. The twenty flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CK) transition.
When the $\overline{OE}$ input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge.
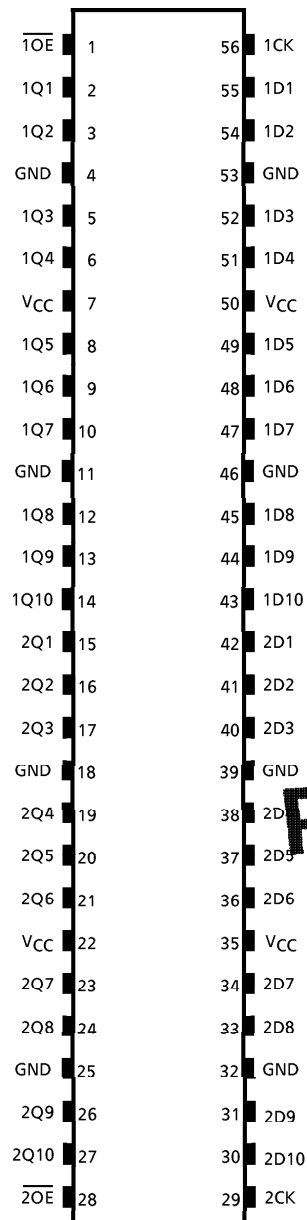

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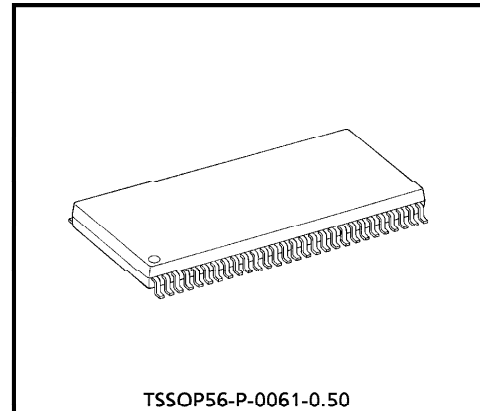
Weight : 0.25g (Typ.)

PRELIMINARY

FEATURES

- Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6V$
- High Speed Operation : $t_{pd} = TBD$ (max.) at $V_{CC} = 3.0 \sim 3.6V$
  : $t_{pd} = TBD$ (max.) at $V_{CC} = 2.3 \sim 2.7V$
  : $t_{pd} = TBD$ (max.) at $V_{CC} = 1.8V$
- 3.6V Tolerant inputs and outputs.
- Output Current   : $I_{OH} / I_{OL} = \pm 24mA$ (min.) at $V_{CC} = 3.0V$
  : $I_{OH} / I_{OL} = \pm 18mA$ (min.) at $V_{CC} = 2.3V$
  : $I_{OH} / I_{OL} = \pm 6mA$ (min.) at $V_{CC} = 1.8V$
- Latch-up Performance : $\pm 300mA$
- ESD Performance   : Human Body Model $> \pm 2000V$
  : Machine Model $> \pm 200V$
- Package   : TSSOP
  (Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.
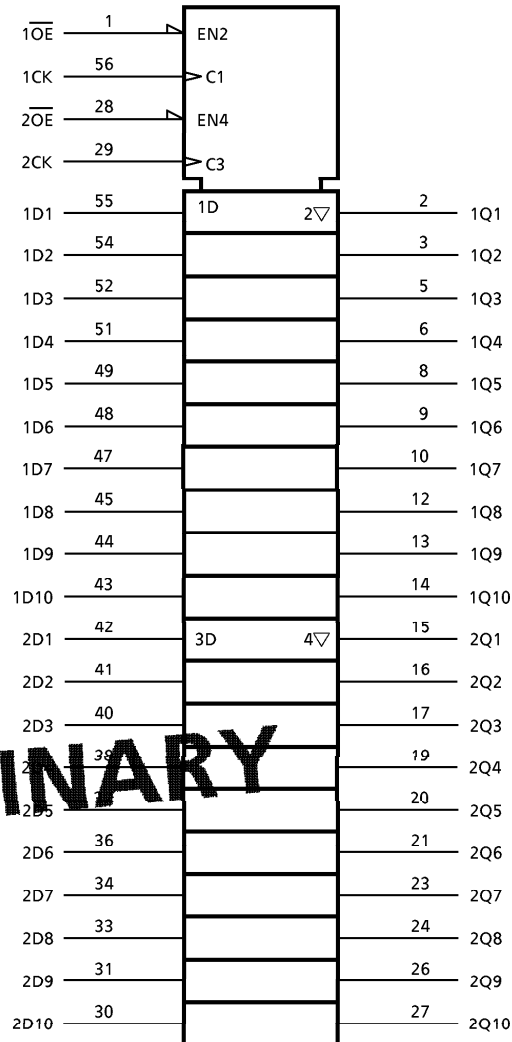
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PIN ASSIGNMENT

$\overline{1OE}$	1	56	1CK
1Q1	2	55	1D1
1Q2	3	54	1D2
GND	4	53	GND
1Q3	5	52	1D3
1Q4	6	51	1D4
V_{CC}	7	50	V_{CC}
1Q5	8	49	1D5
1Q6	9	48	1D6
1Q7	10	47	1D7
GND	11	46	GND
1Q8	12	45	1D8
1Q9	13	44	1D9
1Q10	14	43	1D10
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
V_{CC}	22	35	V_{CC}
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2Q10	27	30	2D10
$\overline{2OE}$	28	29	2CK

(TOP VIEW)

SYMBOL

Input	Pin		
$\overline{1OE}$	1	EN2	
1CK	56	C1	
$\overline{2OE}$	28	EN4	
2CK	29	C3	

1D1	55	1D	2▽	2	1Q1
1D2	54			3	1Q2
1D3	52			5	1Q3
1D4	51			6	1Q4
1D5	49			8	1Q5
1D6	48			9	1Q6
1D7	47			10	1Q7
1D8	45			12	1Q8
1D9	44			13	1Q9
1D10	43			14	1Q10
2D1	42	3D	4▽	15	2Q1
2D2	41			16	2Q2
2D3	40			17	2Q3
2D4	38			19	2Q4
2D5	37			20	2Q5
2D6	36			21	2Q6
2D7	34			23	2Q7
2D8	33			24	2Q8
2D9	31			26	2Q9
2D10	30			27	2Q10

PRELIMINARY

TRUTH TABLE

INPUT			OUTPUT
1$\overline{\text{OE}}$	1CK	1D1-1D10	1Q1-1Q10
H	X	X	Z
L	⌐↓	X	Qn
L	⌐↑	L	L
L	⌐↑	H	H

INPUT			OUTPUT
2$\overline{\text{OE}}$	2CK	2D1-2D10	2Q1-2Q10
H	X	X	Z
L	⌐↓	X	Qn
L	⌐↑	L	L
L	⌐↑	H	H

X : Don't Care
Z : High impedance
Qn : No change

SYSTEM DIAGRAM